

AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1 1. (Original) An integrated circuit comparator comprising:
2 an input receiving an input signal representative of a difference between quantities to be
3 compared; and
4 an input gain stage receiving the input signal and biased with a pulsed bias current, the input
5 gain stage producing a gain based upon the input signal.

1 2. (Original) The integrated circuit comparator according to claim 1, wherein the input signal
2 is a current representative of transconductance of a differential pair of input transistors.

1 3. (Original) The integrated circuit comparator according to claim 1, wherein the input gain
2 stage further comprises a current source biased by the pulsed bias current and controlled by the input
3 signal.

1 4. (Currently Amended) The integrated circuit comparator according to claim 1, further
2 comprising:

3 a voltage limiter and a hysteresis circuit coupled to an output of the input gain stage to reduce
4 spurious output ~~currents~~transitions when the pulsed bias current is not assertedchanges state.

1 5. (Currently Amended) The integrated circuit comparator according to claim 4, further
2 comprising:

3 an output gain stage coupled to the hysteresis circuit and having a gain varying with the
4 ~~gain~~bias change of the input gain stage.

1 6. (Original) The integrated circuit comparator according to claim 4, further comprising:

2 an output gain stage coupled to the hysteresis circuit and having a fixed gain and a
3 propagation delay negligible with respect to a propagation delay of the input gain stage.

1 7. (Original) The integrated circuit comparator according to claim 1, wherein the pulsed bias
2 current comprises a pulse at one edge of a system clock and an output of the comparator is sampled
3 at another edge of the system clock.

1 8. (Currently Amended) The integrated circuit comparator according to claim 1, wherein the
2 comparator selectively operates in a first mode in which the input gain stage is biased by a
3 continuous bias current with a defined first level value or in a second mode in which the input gain
4 stage is biased by the pulsed a bias current with a different second level value.

1 9. (Original) A method of operating an integrated circuit comparator comprising:
2 receiving an input signal representative of a difference between quantities to be compared
3 at an input for the comparator; and
4 transmitting the input signal from the input to an input gain stage biased with a pulsed bias
5 current, the input gain stage producing a gain based upon the input signal.

1 10. (Original) The method according to claim 9, wherein the input signal is a current
2 representative of transconductance of a differential pair of input transistors.

1 11. (Original) The method according to claim 9, wherein the input gain stage further comprises
2 a current source biased by the pulsed bias current and controlled by the input signal.

1 12. (Currently Amended) The method according to claim 9, further comprising:
2 with an output signal from the input gain stage, driving a voltage limiter and a hysteresis
3 circuit coupled to the output of the input gain stage to reduce spurious output ~~currents~~transitions
4 when the pulsed bias current ~~is not asserted~~changes state.

1 13. (Original) The method according to claim 12, further comprising:
2 varying a gain of an output gain stage coupled to the hysteresis circuit with the bias change
3 of the input gain stage.

1 14. (Original) The method according to claim 12, further comprising:
2 fixing a gain of an output gain stage coupled to the hysteresis circuit and having a
3 propagation delay negligible with respect to a propagation delay of the input gain stage.

1 15. (Original) The method according to claim 9, wherein the pulsed bias current comprises a
2 pulse at one edge of a system clock and an output of the comparator is sampled at another edge of
3 the system clock.

1 16. (Original) The method according to claim 9, wherein the comparator selectively operates in
2 a first mode in which the input gain stage is biased by a continuous bias current or in a second mode
3 in which the input gain stage is biased by the pulsed bias current.

1 17. (Original) An integrated circuit comprising:
2 a comparator selectively operating in a first mode in which an input gain stage of the
3 comparator is biased with a pulsed bias current and a second mode in which the input gain stage is
4 biased with a continuous bias current.

1 18. (Original) The integrated circuit according to claim 17, wherein the input gain stage receives
2 an input signal representative of a difference between quantities to be compared and produces a gain
3 based upon a current for the input signal representative of transconductance of a differential pair of
4 input transistors.

1 19. (Original) The integrated circuit according to claim 18, wherein the input gain stage further
2 comprises a current source biased by the pulsed or continuous bias current and controlled by the
3 input signal.

- 1 20. (Currently Amended) The integrated circuit according to claim 19, further comprising:
2 a voltage limiter and a hysteresis circuit coupled to an output of the input gain stage to reduce
3 spurious output ~~currents~~transitions when the pulsed bias current is ~~not asserted~~changes state.